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09/042,417	03/13/1998	GILBERT M. WOLRICH	15311-2107	4956

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EXAMINER

BACKER, FIRMIN

ART UNIT

PAPER NUMBER

2155

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 09

Application Number: 09/042,417
Filing Date: March 13, 1998
Appellant(s): WOLRICH ET AL.

Robert A. Cesari
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 12th, 2001.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

Appellant's brief includes a statement that claims 1-7 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

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(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,684,729	Yamada et al	11-1997
5,627,773	Wolrich et al	5-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,018,756. Although the conflicting claims are not identical, they are not patentably distinct from each other because

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3. The only difference between these two claimed inventions is that in claim 1, the limitation "a normalization-shift-determination circuit that determines a required normalization shift by generating a possible-shift-point-vector signal comprising a plurality of bit signals representing respective bits of a possible-shift-point vector, each bit in the possible-shift-point vector corresponding to a different bit position in the input operands' mantissas, the value of each bit signal in the possible-shift-point vector being determined only from at most three, consecutive bits of the each input operand's mantissa, and applying to the processing trains a normalization-shift signal representing the position of the most-significant one bit in the possible-shift-point vector" is omitted. Clearly, applicant is attempting to obtain a broader coverage in the claim of the application.

4. It is well settled that then omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA 1963). Also note Ex parte Rainu, 168 USPQ 375 (Bd. App 1969). Omission of a reference element whose function is not needed would obvious to one of ordinary skill in the art.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Lynch (U.S. Patent No. 5,901,076).

7. As per claim 1, Lynch teaches an addition pipeline (arithmetic unit), adapted for application of first and second operand signals, each of which represents the sign, exponent, and mantissa of floating-point input operand, for performing an effective addition or subtraction on the input operands and generating an addition-pipeline output signal representing the result (see abstract, fig. 2, 3, and column 1 line 7-10, 4 lines 12-55), the addition pipeline comprising a mantissa adder (adder/subtractor, 110) for application of first and second mantissa signals respective mantissa values (see fig 2, 3, column 4 line 12-55), perform addition and subtraction on the mantissa values and generate a mantissa adder output (see abstract, fig 2, 3, column 2 line 35-3 line 10, 4 line 12-55), mantissa processing circuit for generating and applying mantissa input operands to the mantissa adder, subtracting a pair of mantissas when they are offset to the left by one position from the applied mantissa signals and add when the pair of mantissas are the same (see abstract, fig 2, 3, 4, column 1 lines 25-67, 3 line 35-3 line 10, 4 line 12-55, 6 lines 25-41).

8. As per claims 2, 3 Lynch teaches an addition pipeline wherein the main mantissa adder performs a normalization shift in one direction (to the right only) when necessary to produce an output within predetermined normalization limits capable of performing the normalization shift

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in only one direction (see abstract, fig 2, 3, 4, column 1 lines 25-67, 3 line 35-3 line 10, 4 line 12-55, 6 lines 25-41).

9. As per claim 4, 7, Lynch teaches an addition pipeline wherein the mantissa processing circuitry comprises a pair of processing trains for generating first and second processed mantissa signals from input operands' mantissas, each processing train performing a shift, for at least a plurality of input-operand-value pairs, that is one more position to the left for an effective subtraction than for an effective addition (see abstract, fig 2, 3, 4, column 1 lines 25-67, 3 line 35-3 line 10, 4 line 12-55, 6 lines 25-41).

10. As per claim 5, 6, Lynch teaches an addition pipeline wherein the mantissa adder includes rounding circuit operable in at least one rounding mode to add a rounding bit and being capable of adding the rounding bit at a selected one of only two bit positions in a given rounding mode (see abstract, fig 2, 3, 4, column 1 lines 25-67, 3 line 35-3 line 10, 4 line 12-55, 6 lines 25-41).

(11) Response to Argument

Applicants argue that a feature the reference contains no suggestion that the mantisas be shifted differently prior to a subtraction than an addition. Applicants also argue that there is no suggestion that mantisas-shifting be changed in any way in order to deal with the normalization that may be required after an addition or subtraction operation. Applicants further argue that there is no reference to a difference in the amount of shifting when the operation is a subtraction

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as opposed to addition. Examiner respectfully disagrees with the characterization of the reference. First of all, in applicants' disclosure, there is no mention of mantissas be shifted differently prior to a subtraction than an addition neither a difference in the amount of shifting when the operation is a subtraction as opposed to addition, nor a difference in the amount of shifting when the operation is a subtraction as opposed to addition. In a complete re-assessment of the application, examiner was unable to characterize these limitations pointed by the application, neither in the claim nor in the specification. Applicants seem to be arguing an inventive concept that is unrelated to the disclosure. Nevertheless, the reference (Lynch) clearly teaches the above limitation. Lynch teaches that addition and subtraction operations associated with floating point numbers are somewhat more complicated than addition and subtraction of integer numbers. Before actually performing an addition or subtraction operation upon the mantissas of the numbers, since the numbers are typically normalized, the relative magnitudes of the exponents must be compared to align the mantissas, if necessary. If the two exponents are equal, thus indicating that the mantissas are already aligned, the arithmetic operation can be effectuated by directly adding (or subtracting) the mantissas according to the desired operation. However, if the exponents are not equal, then the mantissa with the smaller exponent is typically shifted to the right by a number of positions equal to the difference between the exponents. Once the mantissas have been aligned, an arithmetic operation of addition or subtraction may be performed upon the aligned mantissas in accordance with the desired operation. Subsequently, post normalization of the result is carried out. It is noted that subtraction may be carried out by two's complementing the subtrahend and performing an addition operation. For the special case in which one of the operands is equal to zero, other specific operations may be performed. Lynch


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further teaches Ripple carry shifters 102 and 104 shift the mantissa of the associated floating point number provided thereto to the right by a number of positions equal to the difference between the exponent values. That is, in this embodiment ripple carry shifter 102 is configured to subtract the exponent value of floating point number FP1 from the exponent value of the floating point number FP2, and to shift the mantissa of floating point number FP1 to the right by a number of positions equal to the calculated difference. Similarly, ripple carry shifter 104 is configured to subtract the exponent value of floating point number FP2 from the exponent value of the floating point number FP1, and to shift the mantissa of the floating point number FP2 by a number of positions to the right equal to the calculated difference. As stated previously, only one of the shifted mantissas is selected by multiplexor 106 for application to an input port of an adder/subtractor 110. The adder/subtractor unit 110 operates upon the unshifted mantissa of the floating point number having the larger exponent and upon the shifted mantissa of the floating point number having the smaller exponent in accordance with the desired operation (i.e., add or subtract), and depending upon the original signs of the numbers, if present. The result from adder/subtractor unit 110 may then be normalized by a normalization unit 112. (see column 4 lines 11-55)

For the above reasons, it is believed that the rejections should be sustained.

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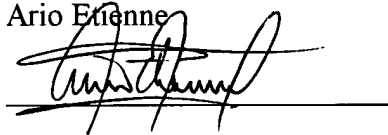
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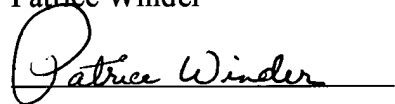
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